Digital Techniques & Digital Systems
Lecturer: Najwa M. Hassan.
Second Year
Theoretical: 2 Hrs. / Week.
CCE 231
Tutorial: 1Hrs./ Week.

## First Term

1. Minimization of Logic Functions:
   - Tabular Method.
   - Bridging Techniques.

2. MSI Functional Circuit:
   - Multiplexers, Demultiplexers, Decoder Encoder, adder (Look-ahead-adder), comparator.
   - The Internal Circuits and Applications in digital design.

3. Sequential Circuit Part I:
   - Study of Memory elements: (Flip-Flops: SR, JK, D and T type).
   - Computer design: (Synchronous, Asynchronous (Ripple), Ring counters, I. C. and Cascaded counters).
   - Shift Register.
4. Memory and Multiple Output Networks:
   ROM, RAM, PLA, PAL and Memory Expansion.

## Second Term

1. I. C.- Technology, Digital Electronics.
   - Introduction to I. C. Classifications (SSI to ULSI).
   - Bipolar and FET Technology.

2. Analog to Digital and Digital to Analog Converters (A/D) & (D/A):
   - Binary weighted and R/2R Ladder D/A.
   - Simultaneous, Stair – Step – Ramp, Single Slope, Dual Slope and Successive Approximation A/D.
3. Sequential Circuit Design:
   - Synchronous Sequential Network:
     - Design using Mealy and Moore model.
     - Analysis and implementation using different types of flip flops as memory elements.
     - The use of SSI, ROM, PAL and PLA in a combinational part design.
     - The use of adjacency rule method for optimal network design.

   - Asynchronous sequential network:
     - Design using Moore and Mealy model.
     - Analysis and design with race-free and ripples free circuits.
     - Implementation of the circuit using SSI, SR-Latches, ROM, PLA and PAL.

References:


- Booth, " Introduction to Computer  Engineering Hardware and Software".
- Roth, "Fundamentals of Logic Design".
- Floyed " Digital Fundamentals".
- Douglas Lewin " Design of Logic Systems".
- Albert Paul Malvino, " Digital Principles and Applications".
- Morris Mano, " Computer Engineering Hardware Design".

## Combination Logic Design

1) Minimization Techniques:

   a) Karnaugh Map (K-Map):for 5 and 6 variables.
   b) Tabular Method (Quine-Mcluskey): for problems with large number of switching variables breaks down. Above six variables K-Map technique becomes two complex, so Tabular method is used. The advantage of this method is that it operates directly on the actual switching terms.
   c) Bridging Technique: This technique make use of the EX- OR function, ANDing or ORing with a function.

2) MSI Functional Circuit:

   a) Multiplexer: a multiplexer or data selector has a group of inputs and a group of control inputs (to select one of the data inputs and connect it to the input terminal).

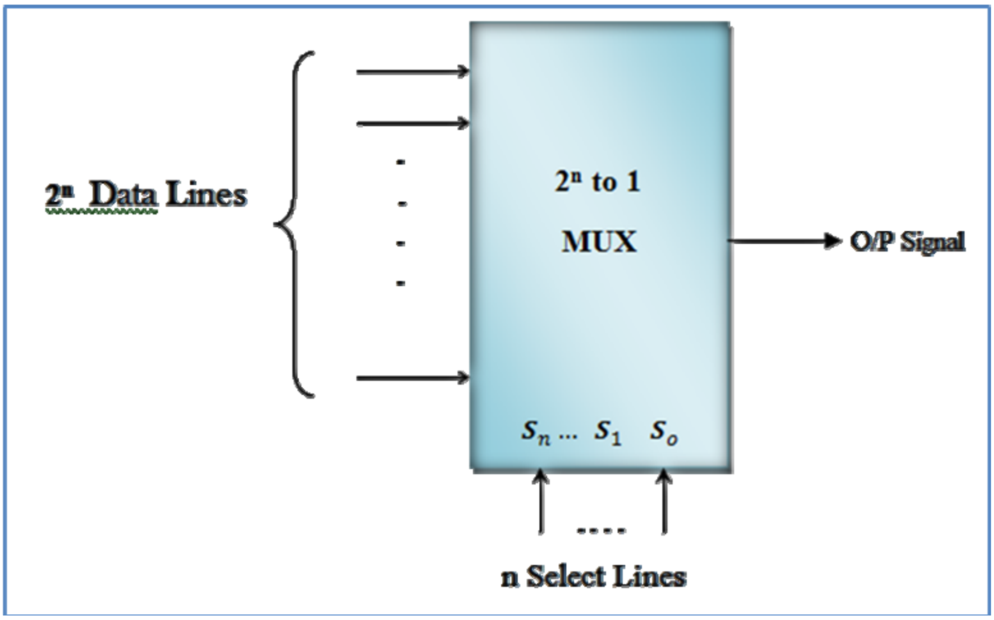



Figure (1): $2^n$ to 1 Multiplexer.

b) Demultiplexer: basically it reverses the multiplexing function; it takes data from one line and distributes them to a given number of output lines.
c) Decoder: its function to detect the presence of specified combination of bits on its output. It has *n* input lines and forms one to $2^n$ output lines and produce 1 or 0 at one and only one output line.

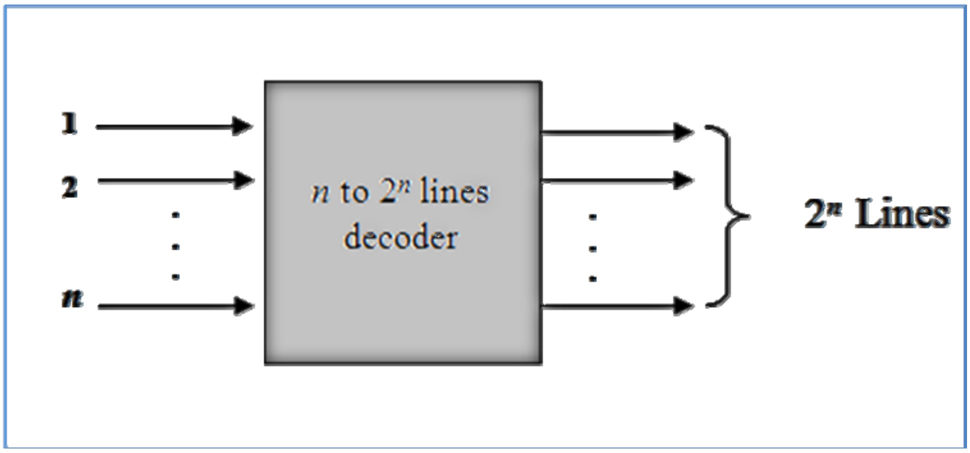



Figure (2):*n* to $2^n$ lines Decoder.

d) Encoder: it performs a reverse decoder function.
e) Priority Encoder: it is a combination circuit that implements the priority function such that it has two or more inputs are equal to logic one at the same time but the highest priority input will take precedence.

3) Read Only Memory (ROM): basically it consists of a Decoder and a memory array as shown in figure (3). When a pattern of *n* 0's and 1's applied to the decoder inputs, exactly one of the $2^n$ Decoder outputs is 1.This decoder output line selects one of the words in the memory array, and the bit pattern stored in this word is transferred to the memory output lines.

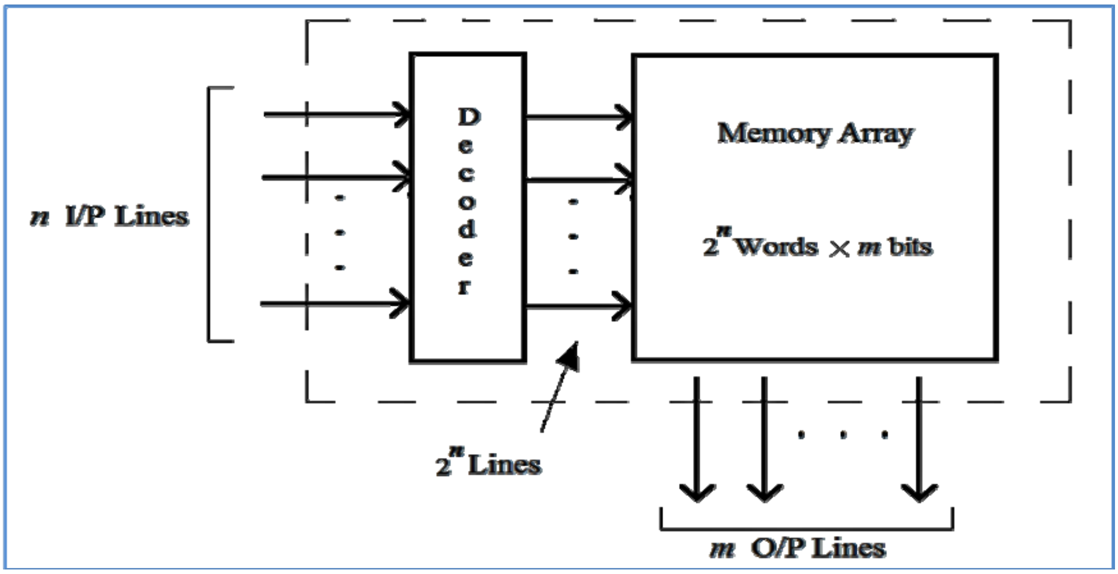



Figure (3): Basic ROM Structure.

4) Programmable Logic Array (PLA): performs the same basic function as a ROM, a PLA with *n* inputs and *m* outputs (as shown in figure (4)) can realize *m* functions of *n* variables. The internal organization of the PLA is different from that of the ROM. The decoder is replaced with AND array which realizes selected product terms of the input variables. The OR array ORs together the product terms to form the output function.

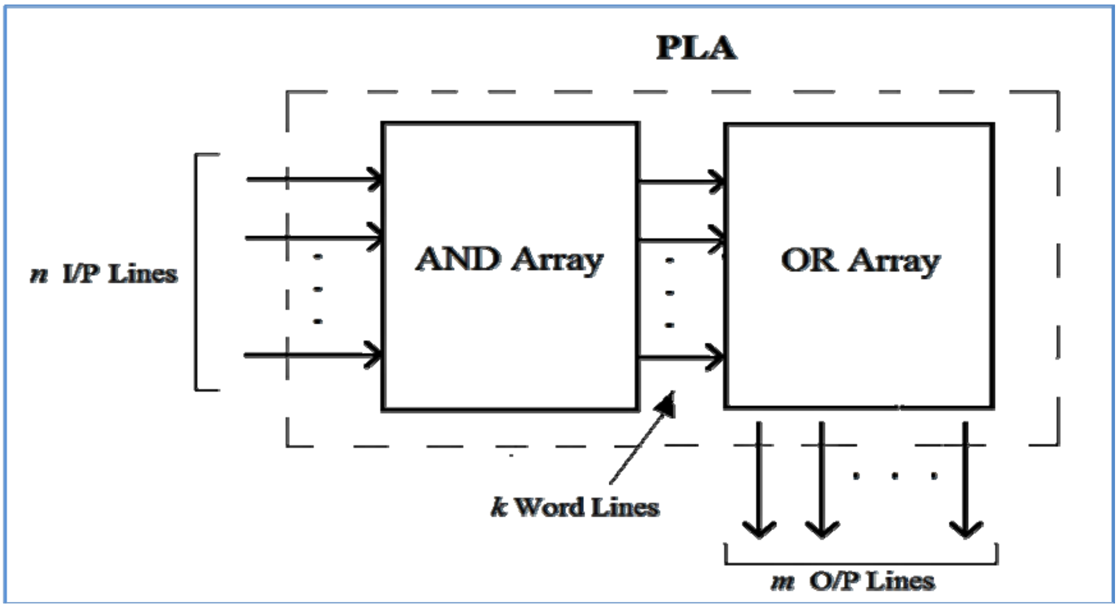



Figure (4): Basic PLA Structure.

5) Flip-Flops (F.F): is a sequential circuit that functions as a basic logic memory element. Basically a flip flop is memory device which can assume one of two stable output states which has a pair of complementary outputs; and which has one or more inputs that can cause the output state to change.

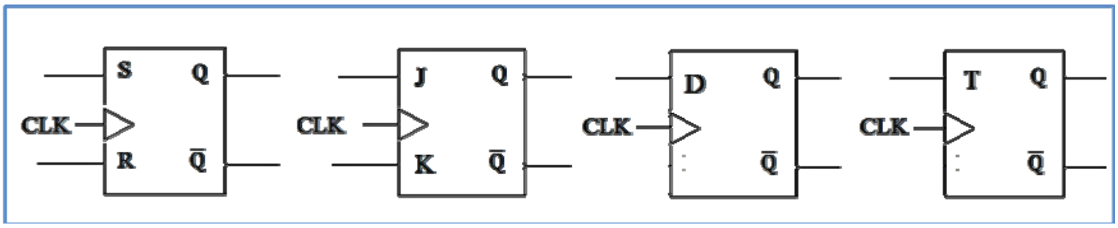



Figure (5): SR, JK, D and T Flip Flops.

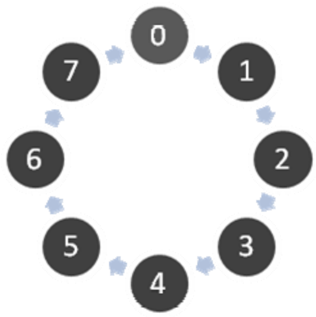
6) Counters: are of the simplest types of the sequential networks. A counter is usually constructed from two or more flip flops which change state in a prescribed sequence when input pulses are received.

a) Synchronous Counters: in this type the operation of flip flops is synchronized by the input pulse so that when the pulse is received several flip flops must change state, the state changes occur simultaneously.

- Binary Counter: is built from n F.Fs, it starts at 0 and count to $2^n - 1$ then reset to 0. A transition diagram and a transition table is given for a binary up counter or module $2^n$ counter.

| Present State | | | Next State | | |
|---|---|---|---|---|---|
| A | B | C | $A^+$ | $B^+$ | $C^+$ |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |

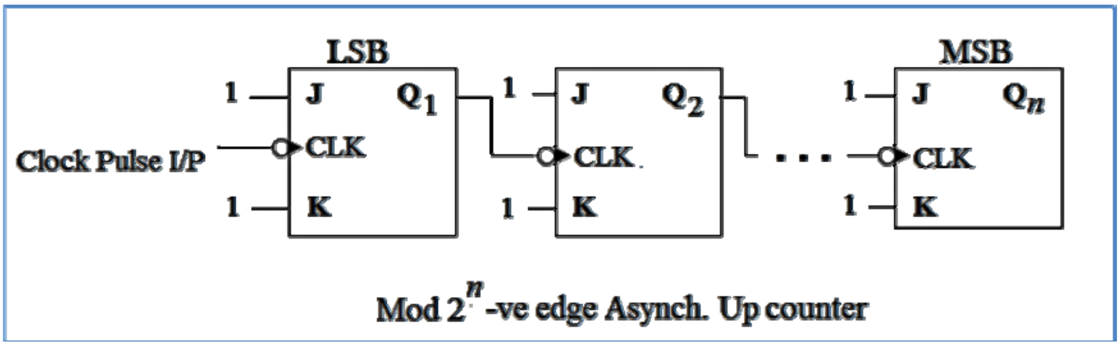
State Table



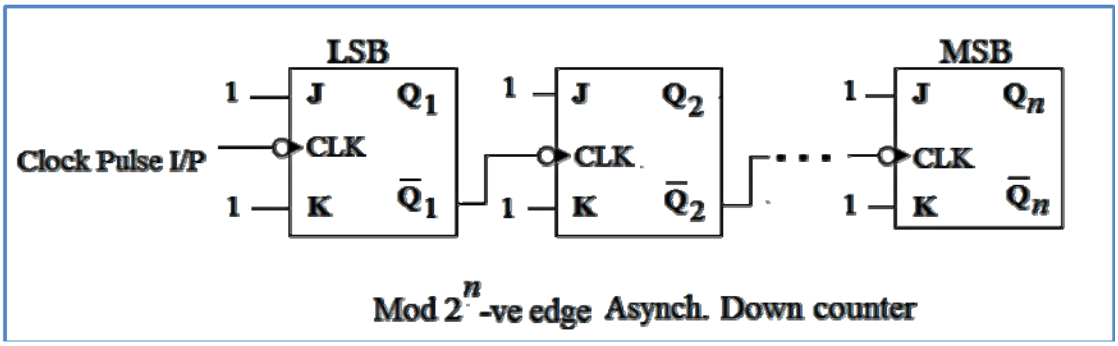

State Diagram n=3

- Non Binary Counter: it does not follow a binary counting sequence like Gray code counter and Excess-3 counter.

b) Asynchronous (Ripple) Counter: in this type the first F.F(Which represents the Least Significant Bit LSB) only receives the clock pulse while the later stages feed each other by the output signal of a F.F to be the clock of the next one. The F.F that are used in this kind of counters should have the toggle state i.e. the input signals are always set to logic one; this means that JK and T F.Fs are used only while other types should be converted to JK or T in order to be used.

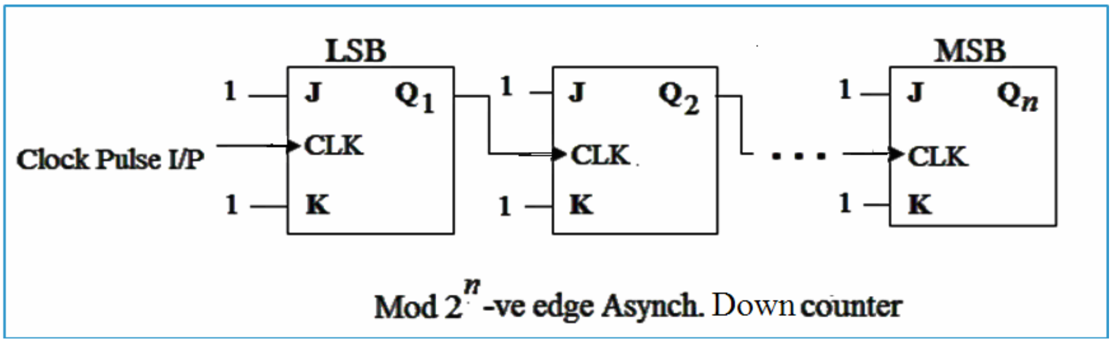



(a)

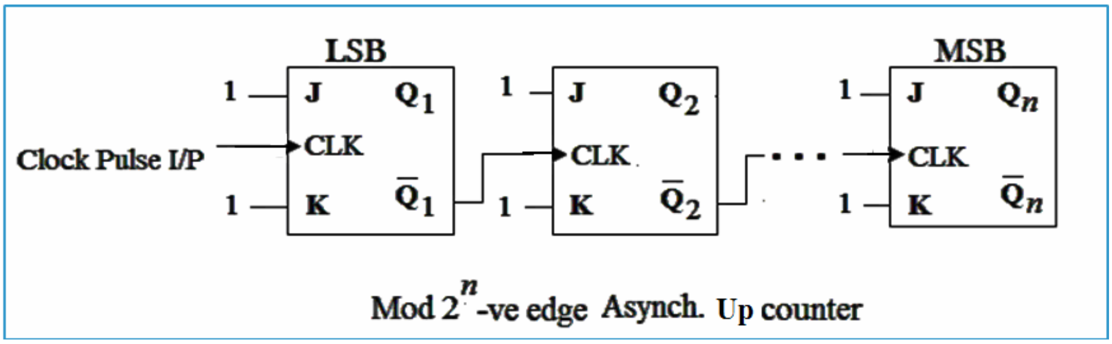



(b)

Figure (6): a- Mod. $2^n$ –ve edge Asynchronous up counter ,b- Mod. $2^n$ –ve edge Asynchronous down counter.




a




b

Figure (7): a- Mod. $2^n$ +ve edge Asynchronous down counter ,b- Mod. $2^n$ +ve edge Asynchronous up counter.

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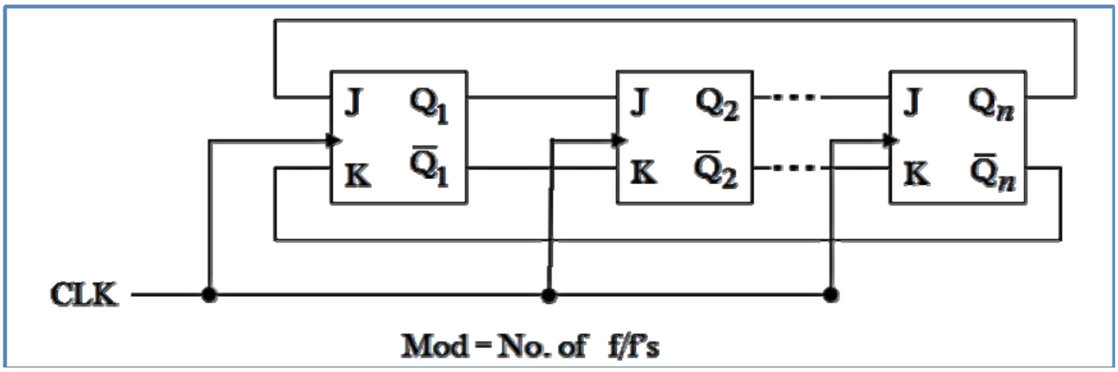
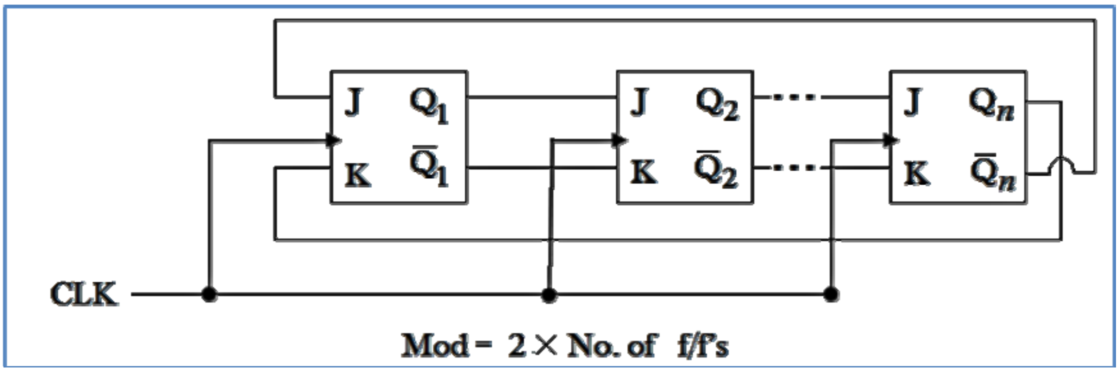
C) Ring Counter: here the "1" is shifted to the next F.F and the "1" is circulated round and round and round as long as the clock pulses applied, hence, the circuit is called a *ring* counter. While the twisted ring counter the last stage outputs are twisted before applying them to the first stage inputs (see figure (7)).




(a)

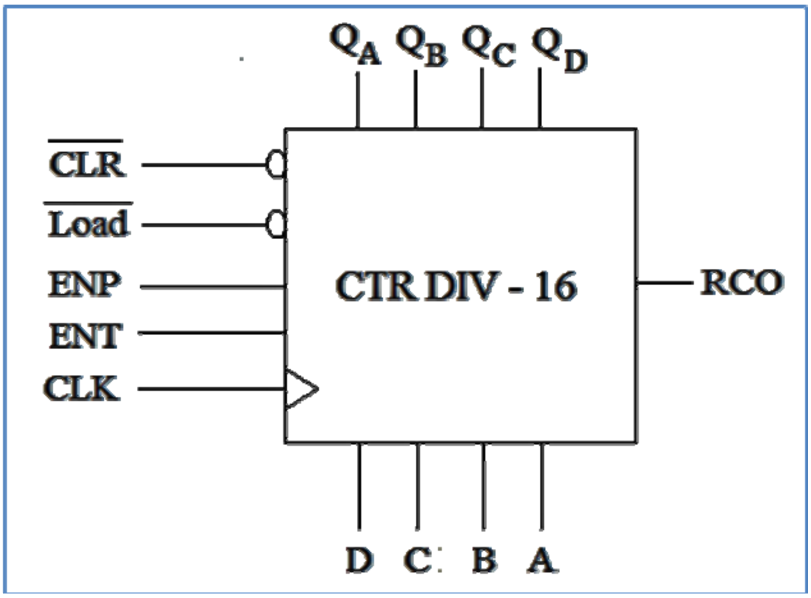



(b)

Figure (8): a- Ring counter, b- Twisted ring counter.

d) Cascade Counters: can be connected in cascade to achieve higher modulus operation.

e) I. C. Counters: such as 74LS160 which is a synchronous decade counter (0-9); and 74S163 mod. 16 counter.




Figure(9): Mod. 16 I.C. Counter.

- $\overline{\text{Load}}$: loading at "0" input, no loading at"1".
- CLR: performs clearing the I.C. at "0", at "1" no operation.
- ENT, ENP: are two enable, when both are "1" count sequence is through binary state, when one of them at least is "0" count is disable.
- RCO: goes "1" when the count is complete (reach $(1111)_H$).